A 2-V OPERATION RF FRONT-END GaAs MMIC FOR PHS HAND-SET

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ABSTRACT

A single 2-V operation RF front-end MMIC has been developed using three kinds of self-aligned gate MESFETs. Its transmitter block of a power amplifier with an antenna switch exhibited a power gain of 28.9 dB and a high power-added efficiency of 27.0 % at 20.5-dBm output power. The receiver block of a low-noise amplifier with the antenna switch exhibits a noise figure of 3.4 dB and a gain of 11.1 dB.

INTRODUCTION

Digital mobile communications have greatly expanded, such as the 1.9-GHz personal handy phone system (PHS). This commercial system demands very compact and low-cost handy phones with longer taking and waiting time. The effective ways to meet these requirements are single-chip integration and lower-voltage operation. As operation voltage is lowered, the power consumption for Si CMOS baseband LSIs is reduced, which are acting even in the standby mode. Although CMOS LSIs currently operate at about 3 V, lower-voltage CMOSs will be surely available in the near future.

This paper describes an RF front-end single-chip GaAs MMIC module for PHS handsets which operates with a single low-2V supply. Figure 1 shows a block diagram of the MMIC, which has a 3-stage power amplifier (PA), a single-pole-double-throw (SPDT) antenna switch (SW) and a single-stage low-noise amplifier (LNA). A new circuit configuration was applied to the SW to realize both sufficient power-handling capability even in low 2-V operation and small chip area.

We used three kinds of planar, refractory WNx/W self-aligned gate MESFETs, as shown in Fig.2, so as to optimize each circuit.

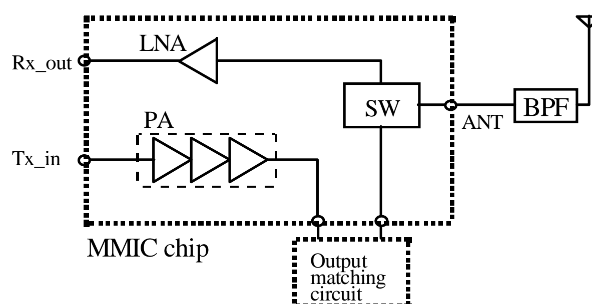

Fig.1 Block diagram of RF front-end MMIC

FET STRUCTURE

Refractory gate technology is a promising approach for power MESFET production because of its simple process, good device reproducibility and reliability. In addition, some devices of which characteristics such as threshold voltage are different can be fabricated easily on a chip, and therefore, this technology is quite suitable for multifunction integration.

The PA comprises 0.8 μm-gate P-pocket MESFETs (Fig.2(a)) to realize high-efficiency operation with a single low 2-V supply[1]. The threshold voltage is about -0.3 V.

The SW comprises 0.6 μm-gate buried P-layer MESFETs with 0.3 μm-offset both at source and drain sides (Fig.2(b)) to obtain low

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on-resistance and high breakdown voltage[2]. The threshold voltage is about -1.2 V.

The LNA comprises 0.6μm-gate asymmetrically self-aligned buried-P-layer MESFET (Fig.2(c)), which has high Gm and contributes to high gain and low noise. The threshold voltage is about -0.4 V.

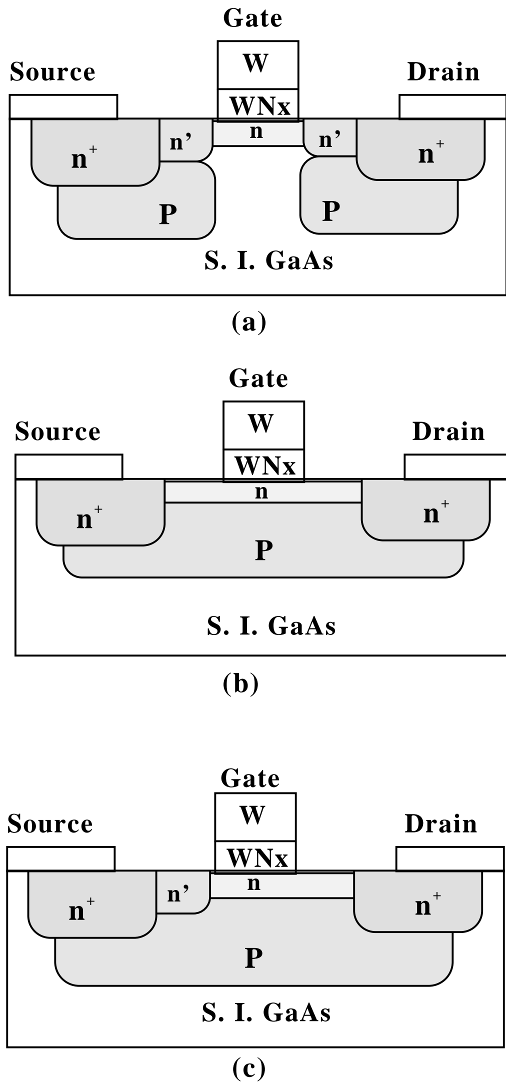

Fig.2 Cross-sectional view of
(a) P-pocket MESFET for PA,
(b) BP-MESFET for SW,
(c) asymmetrically self-aligned BP-MESFET for LNA

CIRCUIT DESIGN

Figure 3 shows a schematic circuit of the three-stage power amplifier.

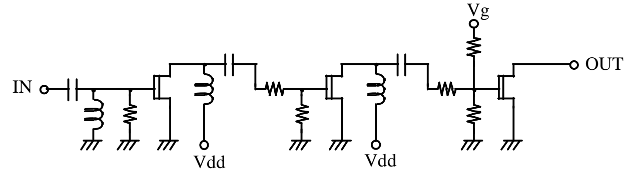

Fig.3 Circuit configuration of the PA

The gate widths of the MESFETs were designed to be 0.4 mm, 1.6 mm and 6.8 mm to achieve an output power of 21 dBm with sufficiently low distortion. The input and interstage matching circuits were included on the chip. The output circuit was designed on the alumina module substrate to decrease the chip area and to reduce the transmission loss and dc voltage drop.

Figure 4 shows the schematic circuit of the SW.

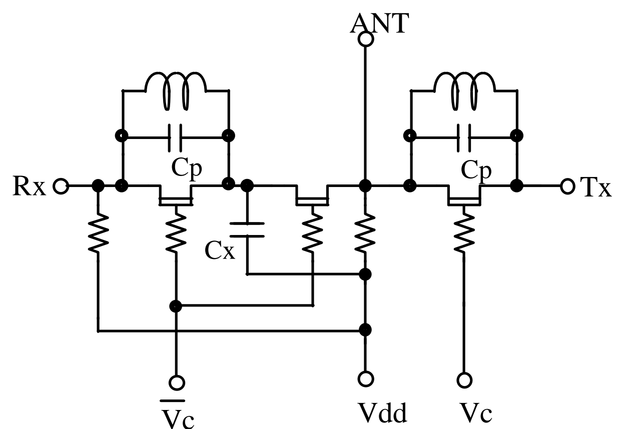

Fig.4 Circuit configuration of the SW

In order to obtain high isolation, we applied a resonant-type configuration which has inductors parallel-connected with FETs. Two stacked FETs and a shunt capacitor Cx at the receiver side are effective for achieving low-

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distortion characteristics[2]. In addition, we have newly introduced parallel capacitors (Cp). Inserting Cp leads to reduction of the layout area for the inductors, and also reduction of the distortion caused by the off-state FET stray capacitance which varies non-linearly with the RF signal voltage. This new circuit configuration enables low-distortion operation at 2-V supply.

Figure 5 shows the schematic circuit of the LNA, which is a self-biased single-stage amplifier. Input and output matching circuits are built on the chip. The bypass capacitor of the self-bias circuit is off-chip.

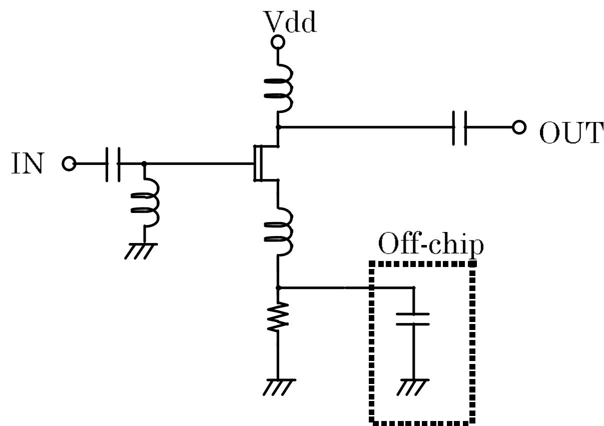

Fig.5 Circuit configuration of the LNA

The MMIC of which the chip size is 1.3 x 3.1 mm was mounted on a lead-less alumina monolayer substrate with capacitor chips and micro-strip transmission lines. Figure 6 shows the top view of the MMIC module without a lid. This MMIC module includes all matching circuits and biasing circuits with high-frequency decoupling capacitors, and its size with the lid is as small as 7.6 x 7.6 x 2.0 mm. In order to realize such small size, we designed the MMIC chip layout and the module substrate pattern concurrently.

RF PERFORMANCE

Figure 7 shows output power characteristics at 2 V in the transmitter block of the PA with the SW. An output power (Pout) of 20.5 dBm and a power gain of 28.9 dB were measured at the antenna port, when adjacent channel leakage power (ACP) was as low as -55 dBc at 600 kHz apart from 1.9 GHz. A high power-added efficiency (PAE) of 27.0 % was attained.

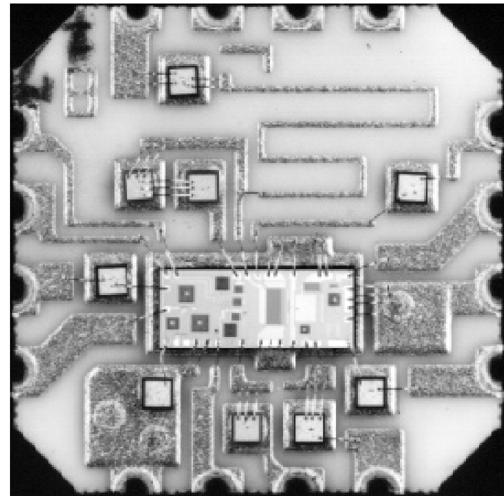

Fig.6 Microphotograph of the MMIC module (module size: 7.6 x 7.6 mm)

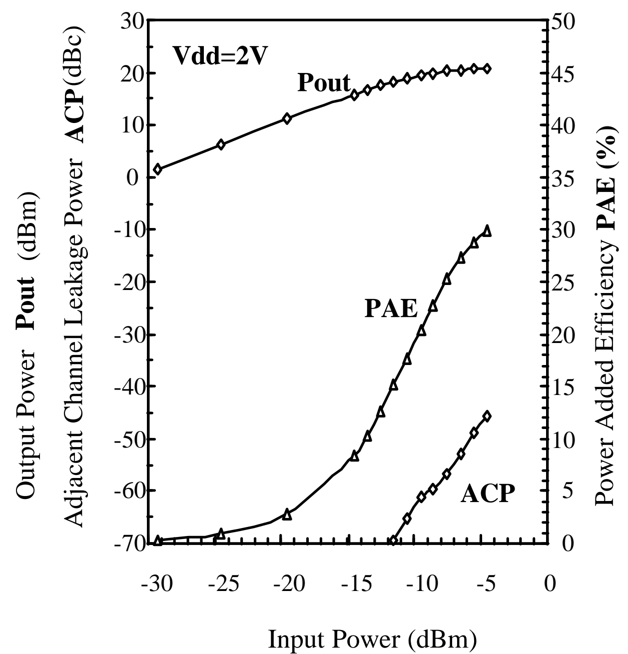

Fig.7 Output characteristics of transmitter block (PA+SW)

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Figure 8 shows frequency characteristics of noise figure (NF) and gain in the receiver block of the LNA with the SW. The receiver block has a noise figure of 3.4 dB and a gain of 11.1 dB. Its dissipation current was as low as 2.05 mA.

We evaluated individual characteristics of the SW and the LNA by fabrication of experimental modules for them.

The small-signal insertion losses of the SW were 0.89 dB and 1.52 dB in the transmitting and receiving modes, respectively. Its small-signal isolations were 35.4 dB and 29.0 dB in the transmitting and receiving modes, respectively.

The experimental module of the LNA exhibits a noise figure of 1.7 dB.

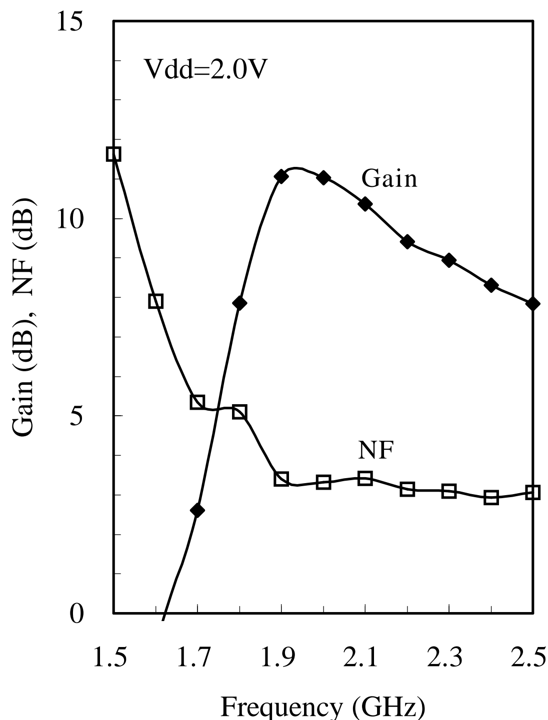

Fig.8 Small-signal characteristics of receiver block(SW+LNA)

CONCLUSION

An RF front-end single-chip MMIC module for PHS handsets has been demonstrated. Despite a small size of 7.6 x 7.6 x 2.0 mm, the module includes all matching and biasing circuits. Single 2-V supply operation was enabled by applying three kinds of planar, self-aligned gate MESFETs and a newly proposed SW circuit configuration. Its transmitter block exhibited a high PAE of 27.0 % at 20.5-dBm output power, and the receiver block operated with a low noise figure of 3.4 dB and a high gain of 11.1 dB. Thus, this MMIC module is expected to contribute greatly to the realization of very compact, low-power and low-cost PHS handsets.

ACKNOWLEDGMENT

The authors wish to thank N. Kurihara, S. Gima, T. Inoue, T. Sawada, Y. Ikeda, H. Nagasawa for their technical contributions. The authors would also thank some good supports of the members of the process and fabrication team.

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